CLAIMS:

1. A static random access memory cell comprising:

a first p-channel pullup transistor having a gate, drain, and source;

a first n-channel pulldown transistor having a gate, drain, and source;

a second p-channel pullup transistor having a gate, drain, and source;

a second n-channel pulldown transistor having a gate, drain, and source; the source of the first pullup transistor being adapted to be connected to a first voltage; the source of the second pullup transistor being adapted to be connected to the first voltage; the drain of the first pulldown transistor being connected to the drain of the first pullup transistor; the drain of the second pulldown transistor being connected to the drain of the second pullup transistor; the source of the first pulldown transistor being adapted to be connected to a second voltage lower than the first voltage; the source of the second pulldown transistor being adapted to be connected to the second voltage; the gate of the first pullup transistor being connected to the gate of the first pulldown transistor; the gate of the second pullup transistor being connected to the gate of the second pulldown transistor; the first pullup transistor and the first pulldown transistor together defining a first invertor having an output defined by the drain of the first pulldown transistor and an input defined by the gate of the first pulldown

transistor, the second pullup transistor and the second pulldown transistor together defining a second invertor having an output defined by the drain of the second pulldown transistor and an input defined by the gate of the second pulldown transistor, the input of the first invertor being connected to the output of the second inverter, and the input of the second invertor being connected to the output of the first invertor; and

a p-channel isolation transistor connected between the drain of the first pullup transistor and the drain of the second pullup transistor, and having a gate.

2. A static random access memory cell in accordance with claim 1 wherein the source of the first p-channel transistor is connected to the source of the second p-channel transistor, and to the gate of the p-channel isolation transistor.

3. A static random access memory cell in accordance with claim 1 wherein the p-channel isolation transistor comprises an active area that is common to both the first pullup transistor and the second pullup transistor.

4. A static-random access memory cell in accordance with claim 1 wherein the source of the first pullup transistor is connected to the first voltage, wherein the source of the second pullup transistor is connected to the first voltage, wherein the source of the first pulldown transistor is connected to the second voltage, wherein the gate of the p-channel isolation transistor is connected to the first voltage, and wherein the source of the second pulldown transistor is connected to the second voltage.

5. A static random access memory cell in accordance with claim 1 wherein the p-channel isolation transistor comprises an active area that is common to both the drain of the first pullup transistor and the drain of the second pullup transistor.

6. A static random access memory cell in accordance with claim 1 and further comprising a first bit line; a second bit line; a word line; a first access transistor having a first active terminal connected to the output of the first invertor, having a second active terminal connected to the first bit line, and having a gate adapted to be connected to the word line; and a second access transistor having a first active terminal connected to the output of the second invertor, having a second active terminal connected to the second bit line, and having a gate connected to the word line.

7. A static random access memory cell comprising:

a first invertor including a first p-channel pullup transistor, and a first n-channel pulldown transistor in series with the first p-channel pullup transistor;

a second invertor including a second p-channel pullup transistor, and a second n-channel pulldown transistor in series with the second n-channel pullup transistor, the first invertor being cross-coupled with the second invertor, the first and second pullup transistors sharing a common active area;

a first access transistor having an active terminal connected to the first invertor;

a second access transistor having an active terminal connected to the second invertor; and

an isolator isolating the first pullup transistor from the second pullup transistor.

8. A static random access memory cell in accordance with claim 7 wherein the first and second pullup transistors have respective gates, wherein the common active area is shared by the gates of the first and second pullup transistors, and wherein the isolator isolates the gate of the first pullup transistor from the gate of the second pullup transistor.

9. A static random access memory cell in accordance with claim 7 wherein the isolator comprises an isolation gate adapted to be biased to isolate the first pullup transistor from the second pullup transistor.

10. A static random access memory cell in accordance with claim 9 wherein the isolation gate cooperates with the active area to define a p-channel transistor.

11. A static random access memory cell in accordance with claim 10 wherein the gate of the isolator is connected to a voltage effective to tri-state the transistor.

12. A static random access memory cell in accordance with claim 9 wherein the isolation gate cooperates with the active area to define a p-channel transistor, the gate of the isolator being connected to a positive voltage.

13. A static random access memory cell in accordance with claim 8 wherein the first invertor has an output, and the active terminal of the first access transistor is connected to the output of the first invertor; and wherein the second invertor has an output, and the active terminal of the second access transistor is connected to the output of the second invertor.

14. A method of manufacturing a static random access memory cell including first and second cross-coupled invertors, each invertor including a p-channel transistor connected in series with an n-channel transistor, the p-channel transistors having sources that are connected to each other and that are adapted to be connected to a common first voltage, and the p-channel transistors having respective drains; the n-channel transistors having respective sources that are connected to each other and that are adapted to be connected to a common second voltage, lower than the first voltage, and the n-channel transistors having respective drains; the method comprising the following steps:

providing a silicon substrate;

defining the first and second invertors relative to the substrate such that the first and second invertors include an active area common to drains of the p-channel transistors; and

defining an isolation gate relative to the common active area, between the drains of the p-channel transistors.

15. A method of manufacturing a static random access memory cell in accordance with claim 14 wherein the step of defining the isolation gate comprises using polysilicon to define the gate.

16. A method of manufacturing a static random access memory cell in accordance with claim 14 and further comprising the step of connecting the sources of the p-channel transistors to the first voltage, connecting the sources of the n-channel transistors to the second voltage, and connecting the isolation gate to a voltage higher than the second voltage.

17. A method of manufacturing a static random access memory cell in accordance with claim 14 and further comprising the step of connecting the isolation gate to the first voltage.

18. A method of manufacturing a static random access memory cell in accordance with claim 14 wherein the step of defining the isolation gate comprises forming polysilicon on the common active area.

19. A method of manufacturing a static random access memory cell in accordance with claim 14 wherein the first invertor has an output, and wherein the second invertor has an output, and further comprising the step of defining a first access transistor having a first active terminal connected to the output of the first invertor, having a second active terminal adapted to be connected to a first bit line, and having a gate adapted to be connected to a word line; and defining a second access transistor having a first active terminal connected to the output of the second invertor, having a second active terminal adapted to be connected to a second bit line, and having a gate adapted to be connected to the word line.

20. A method of manufacturing a wafer including a plurality of static random access memory cells, each cell including first and second cross-coupled invertors, each invertor including a p-channel transistor connected in series with an n-channel transistor, the p-channel transistors having sources that are connected together and that are adapted to be connected to a common first voltage, and having respective drains; the n-channel transistors having sources that are connected together and that are adapted to be connected to a common second voltage, lower than the first voltage, and having respective drains; the method comprising the following steps:

providing a silicon substrate;

defining active areas relative to the substrate for the static random access memory cells, the active areas including an active area having the general shape of a stepladder, including two parallel, spaced apart sides, and a plurality of parallel, spaced apart portions extending between the sides, such that the sides define drains of a plurality of the p-channel transistors; and

defining respective isolation gates relative to active areas, between the drains of the p-channel transistors within each static random access memory cell.

21. A method of manufacturing a wafer in accordance with claim 20 wherein the step of defining the isolation gates comprises using polysilicon to define the gates.

22. A method of manufacturing a wafer in accordance with claim 20 and further comprising the step of connecting the sources of the p-channel transistors to the first voltage and connecting the sources of the n-channel transistors to the second voltage.

23. A method of manufacturing a wafer in accordance with claim 22 and further comprising the step of connecting the isolation gates to a voltage higher than the second voltage.

24. A method of manufacturing a wafer in accordance with claim 22 and further comprising the step of connecting the isolation gates to the first voltage.

25. A method of manufacturing a wafer in accordance with claim 22 wherein the step of defining the isolation gates comprises forming polysilicon on the active area between the drains of the p-channel transistors of each static random access memory cell.

26. A method of manufacturing a wafer in accordance with claim 22 wherein, for each static random access memory cell, the first invertor has an output, and the second invertor has an output, the method comprising the step of defining a first access transistor, for each static random access memory cell, having a first active terminal connected to the output of the first invertor of that cell, having a second active terminal adapted to be connected to a bit line, and having a gate adapted to be connected to a word line; and defining a second access transistor, for each static random access memory cell, having a first active terminal connected to the output of the second invertor of that cell, having a second active terminal adapted to be connected to a bit line different from the first mentioned bit line, and having a gate adapted to be connected to the word line.